REMARKS

This responds to the Office Action mailed on May 17, 2006, and the references cited therewith.

By this response, claims 21, 25, 27, and 34-36 are amended, claims 23-24 and 28-29 are cancelled, and claims 37-44 is added. The amendment to claim 21 corrects some grammatical errors and substantially incorporates the limitations of cancelled claims 23-24. The amendment to claim 25 clarifies a grammatical construction without otherwise changing the claim. The amendment to claim 27 corrects some grammatical errors and substantially incorporates the limitations of cancelled claims 28-29. As a result, claims 1-22, 25-27 and 30-44 are pending in this application (40 total claims (4 additional total claims) and 4 independent claims (2 additional independent claim)). New claims 37-40 are supported by Figure 1 and the description thereof. New claims 41-44 are supported by Figure 2 and the description thereof. No new matter is added. Please charge any added-claim fees to Deposit Account No. 19-0743. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

In view of the following remarks, reconsideration of the rejections and allowance of the claims are respectfully requested.

§102 Rejection of the Claims

A. Rejection: Claims 1-2, 5-13 and 16-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kolichtchak (US 2003/0014667). Applicant respectfully traverses.

B. Response: Applicant's recitation of the law in the response filed February 27, 2006 regarding anticipation is incorporated herein by reference.

The Examiner argues that the Kolichtchak User/Supervisor (U/S) flag serves as an execute/non-execute (X) indicator of the present invention. Applicant disagrees. As is well known in the art (for example, see page 470 of Hennessy and Patterson "Computer Architecture, A Quantitative Approach," Morgan Kaufman Publishers, an imprint of Elsevier Science, San Francisco, CA, © 1990, 1996, 2003), a computer may (1) implement a user mode and an operating-system (e.g., supervisor) mode, (2) provide a portion of the CPU state that the user

process can use but not write (in order to control address-range checks, supervisor privileges, and the like, and (3) provide mechanisms where the CPU can go from user mode to supervisor mode (e.g., by a *system call*, a special instruction that transfers control (i.e., begins executing instructions from) supervisor code space, and when finished, returns to user mode (i.e., resumes executing instructions) similar to a subroutine return that restores the prior user/supervisor mode. Further, well known prior-art read-only protection (i.e., read only versus read and write, e.g., an R/RW flag), when combined with the U/S flag, allows the address translation hardware to detect and prevent certain stray memory accesses. However, Kolichtchak forces all writable pages to be supervisor-mode pages (see Kolichtchak paragraph [0027] 2nd sentence), which cause exceptions (i.e., forced branches to kernel/supervisor code used to kill user processes that try to access supervisor memory) if executed or otherwise accessed in user-mode code (see Kolichtchak paragraph [0011] last sentence) (in Kolichtchak's system, he calls user access to Supervisor data = a page fault, but in any case an exception handler is invoked). When a user-mode process needs valid access to such a writable page (which in normal systems should be marked User&Writable), the access causes an exception and the exception handler temporarily clears the Supervisor flag in its Page Table Entry ("PTE", see Kolichtchak paragraph [0033]), preferably sets the dirty and accessed flags in the PTE, invalidates the TLB entry, which forces the TLB data to be re-fetched to refresh the DTLB record. Then preferably the method again sets the Supervisor flag in the PTE soon after the accessing step.

In Kolichtchak's system, the U/S and R/RW flags are used unconventionally, causing legacy code to be changed/replaced by code that implements the additional checking (4 additional checks in Figure 4A before the original page-fault handler is called) and additional manipulation of the S-flag (reset S 460 to U mode, invalidate TLB 465, refresh DTLB 470, and set S-flag 475). This additional manipulation is apparently required on every user-mode access to any data on a writable page.

Further, Kolichtchak's U/S-flag is not an execute/non-execute bit, since if Kolichtchak's U/S-flag is marked Supervisor and the processor is in Supervisor mode, it does not cause the ITLB to refuse to allow instructions to be loaded or executed. Also, when Kolichtchak's U/S-flag is marked User, instruction execution from that page is allowed even if the page is writable

(since user code (which is supposed to be in read-only (not RW) user-mode pages) is executable if somehow instructions from a U&RW page were fetched—no exception is caused).

Further yet, in Kolichtchak's system, he admits his security can cause a 5% (more or less) performance penalty due to the required switching of a writable page from supervisor mode to user mode each time a user-mode program needs to access (read or write) that writable page. Execution of instructions from the writable page by a user-mode program is prevented because all writable pages are Supervisor-mode pages, and execution from Supervisor-mode pages by user-mode processes causes an exception interrupt. The Kolichtchak S-flag can do nothing to prevent execution of S-mode pages by S-mode programs, even if the pages are accessed in a mode that allows writing

In contrast, independent claim 1 recites "...an executable/non-executable (x) indicator associated with each page in memory wherein the TLB miss handler sets the x-indicator for a particular page to indicate "non-executable" when that page is accessed in a mode that allows writing to that page, and wherein the ITLB refuses to allow instructions from a page with an associated x-indicator of "non-executable" to be loaded." This does not require setting an S-bit on all writable pages, nor a supervisor exception and the performance penalty incurred every time a user-mode program accesses a writable page (which are the case for Kolichtchak's system).

The Kolichtchak reference fails to teach the executable/non-executable (X) indicator as claimed. The present executable/non-executable (X) indicator is set to NON-EXECUTE when a particular page is accessed in a mode that allows writing and refuses to allow instructions from the page to be executed from a page marked non-executable. The Kolichtchak S-flag can do nothing to prevent execution of S-mode pages by S-mode programs, even if the pages are accessed in a mode that allows writing.

In the invention of claim 1, for example, the ITLB refuses to allow instructions from a page with an associated x-indicator of "non-executable" to be loaded. In Kolichtchak, the page fault (exception) handler terminates any user program that tries to execute supervisor-mode instructions, but does not prevent instructions of supervisor-mode programs from being loaded when in supervisor mode (see [0029]). Simply put, the Kolichtchak reference fails to disclose every element of the challenged claim, and fails to disclose the identical invention in as complete

detail as is contained in the claim. Consequently, the Examiner has failed to set forth a proper *prima facie* case of anticipation. Accordingly, this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Claims 2 and 6 and 8 depend from claim 1 and include the recitations of claim 1 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and these claims appear to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Regarding claims 5 and 9, the Kolichtchak reference describes PTE attributes that "include a present attribute P, a read/write flag R/W; and a user/supervisor flag U/S." Kolichtchak does not describe "a read bit indicating that the page is valid and readable; and a write bit indicating that the page is valid and writable" as recited in claim 5. Kolichtchak does not describe "a write bit in each page table entry; and a read bit in each page table entry" as recited in claim 9. Further, these claims depend from claim 1 and include the recitations of claim 1 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and these claims appear to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Regarding claim 7, and further regarding claims 8 and 9, the Kolichtchak reference describes PTE attributes that "include a present attribute P, a read/write flag R/W; and a user/supervisor flag U/S." Kolichtchak does not describe "the x-indicator for each page is held in the page table entry associated with that page" as recited in claim 7. Further, this claim depends from claim 1 and includes the recitations of claim 1 by its dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Independent claim 10 recites 'an executable/non-executable x-indicator associated with each page in memory wherein the DTLB miss handler sets the x-indicator for a particular page to indicate "non-executable" when that page is accessed in a mode that allows writing to that page, and wherein the ITLB refuses to load instructions from a page if the x-indicator indicates a "non-executable" state.' The Kolichtchak reference fails to teach the executable/non-executable (x) indicator as claimed. If, as the Examiner argues, Kolichtchak's U/S-flag indicates non-

executable if in S state, then supervisor code could not execute even in supervisor mode. The Kolichtchak reference indicates otherwise: paragraph [0029] indicates that if in supervisor mode, the original page fault handler is used, and the original page fault handler allows instructions to be loaded for supervisor-mode processes. Consequently, the Examiner has failed to set forth a proper *prima facie* case of anticipation for claim 10, since the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Claims 11-13 and 16-20 depend from claim 10 and include the recitations of claim 10 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claim 11: if, as the Examiner asserts, Kolichtchak's U/S-flag means non-executable if in the S-mode, there is no indication in the reference that Kolichtchak's "ITLB-miss handler sets" this flag 'to an "executable" state [i.e., U-mode, according to the Examiner] when a page is valid and executable.' Further, this claim depends from claim 10 and includes the recitations of claim 10 by its dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claims 16 and 19, the Kolichtchak reference describes PTE attributes that "include a present attribute P, a read/write flag R/W; and a user/supervisor flag U/S." Kolichtchak does not describe "a read bit indicating that the page is valid and readable; and a write bit indicating that the page is valid and writable" as recited in claim 16. Kolichtchak does not describe "a write bit in each page table entry; and a read bit in each page table entry" as recited in claim 19. Further, these claims depend from claim 10 and include the recitations of claim 10 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and these claims appear to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claim 17, and thus also further regarding claims 18 and 19, the Kolichtchak reference describes PTE attributes that "include a present attribute P, a read/write flag R/W; and a user/supervisor flag U/S." Kolichtchak does not describe "the x-indicator for each page is held in the page table entry associated with that page" as recited in claim 17.

Further, these claims depend from claim 10 and include the recitations of claim 10 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Independent claim 21 (a method claim) as amended recites "translating an address for a data access, wherein the translating of the address for the instruction fetch includes determining whether the address has an executable indication associated with the address and then only if executable continuing with the instruction fetch, and is done differently than the translating of the address for the data access, and wherein the translating of the address for the data access includes setting a non-executable indication." The Kolichtchak reference fails to teach that translating of the address for the data access includes setting a non executable indication and that translating of the address for the instruction fetch includes determining whether the address has an executable indication associated with the address and then only if executable continuing with the instruction fetch, as recited in claim 21. Instead. the Kolichtchak reference sets "U" for user addresses, or "S" for supervisor addresses, causes a page fault if in user mode and trying to execute from S-mode addresses but Kolichtchak inherently allows execution of instructions from S-mode addresses if in supervisor mode. Thus, Kolichtchak fails to disclose every element of the challenged claim, and fails to disclose the identical invention in as complete detail as is contained in the claim. Accordingly, claim 21 overcomes the Examiner's rejection under 35 U.S.C. § 102(e) for anticipation by Kolichtchak.

Claims 22, 25, and 26 depend from claim 21 and include the recitations of claim 21 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed. Accordingly, claims 22, 25, and 26 now overcome the Examiner's rejection under 35 U.S.C. § 102(e).

Independent claim 27 (a computer program product claim) as amended includes the same recitation set forth from claim 21 above, but in combination with a computer-usable medium. Thus claim 27 also recites "translating an address for a data access, wherein the translating of the address for the instruction fetch includes determining whether the address has an executable indication associated with the address and then only if executable continuing with the instruction

fetch, and is done differently than the translating of the address for the data access, and wherein the translating of the address for the data access includes setting a non-executable indication." The Kolichtchak reference fails to teach that translating of the address for the data access includes setting a non executable indication and that translating of the address for the instruction fetch includes determining whether the address has an executable indication associated with the address and then only if executable continuing with the instruction fetch, as recited in claim 27. Instead. the Kolichtchak reference sets "U" for user addresses, or "S" for supervisor addresses, causes a page fault if in user mode and trying to execute from S-mode addresses but Kolichtchak inherently allows execution of instructions from S-mode addresses if in supervisor mode. Thus, Kolichtchak fails to disclose every element of the challenged claim, and fails to disclose the identical invention in as complete detail as is contained in the claim. Accordingly, claim 27 overcomes the Examiner's rejection under 35 U.S.C. § 102(e) for anticipation by Kolichtchak.

Claims 30-31 depend from claim 27 and include the recitations of claim 27 by their dependency. Thus, the Kolichtchak reference fails to disclose the invention recited in claims 30-31. Accordingly, claims 30-31 now overcome the Examiner's rejection under 35 U.S.C. § 102(e).

MPEP 2106 Requirements in interpreting means-plus-function claims:

"Where means plus function language is used to define the characteristics of a machine or manufacture invention, claim limitations must be interpreted to read on only the structures or materials disclosed in the specification and "equivalents thereof." (Two en banc decisions of the Federal Circuit have made clear that the Office is to interpret means plus function language according to 35 U.S.C. 112, sixth paragraph. In the first, *In re Donaldson*, 16 F.3d 1189, 1193, 29 USPQ2d 1845, 1848 (Fed. Cir. 1994), the court held:

> The plain and unambiguous meaning of paragraph six is that one construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure. Paragraph six does not state or even suggest that the PTO is exempt from this mandate, and there is no legislative history indicating that Congress intended that the PTO should be. Thus, this court must accept the plain and precise language of paragraph six.

Consistent with *Donaldson*, in the second decision, *In re Alappat*, 33 F.3d 1526, 1540, 31 USPQ2d 1545, 1554 (Fed. Cir. 1994) (in banc), the Federal Circuit held:

> Given Alappat's disclosure, it was error for the Board majority to interpret each of the means clauses in claim 15 so broadly as to "read on any and every means for performing the function" recited, as it said it was doing, and then to conclude that

> claim 15 is nothing more than a process claim wherein each means clause represents a step in that process. Contrary to suggestions by the Commissioner, this court's precedents do not support the Board's view that the particular apparatus claims at issue in this case may be viewed as nothing more than process claims.
>
> Disclosure may be express, implicit or inherent. Thus, at the outset, Office personnel must attempt to correlate claimed means to elements set forth in the written description. The written description includes the original specification and the drawings. Office personnel are to give the claimed means plus function limitations their broadest reasonable interpretation consistent with all corresponding structures or materials described in the specification and their equivalents including the manner in which the claimed functions are performed. See *Kemco Sales, Inc. v. Control Papers Company, Inc.*, 208 F.3d 1352, 54 USPQ2d 1308 (Fed. Cir. 2000). Further guidance in interpreting the scope of equivalents is provided in MPEP § 2181 through § 2186.
>
> While it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. An applicant can always amend a claim during prosecution to better reflect the intended scope of the claim.
>
> Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered. See, e.g., *Diamond v. Diehr*, 450 U.S. at 188-89, 209 USPQ at 9 ("In determining the eligibility of respondents' claimed process for patent protection under 101, their claims must be considered as a whole. It is inappropriate to dissect the claims into old and new elements and then to ignore the presence of the old elements in the analysis. ...").

Means-plus-function claim 32 recites "...means for translating addresses for instructions; means for translating addresses for data, wherein means for translating addresses for instructions operates separately from means for translating addresses for data, and wherein means for translating the address of a page for a data access further includes means for setting a non executable indication." The Examiner has not cited equivalent structures, material, or acts described therein (for translating addresses for the data versus translating addresses for instructions) to perform the functions as recited in claim 32. Consequently, the Examiner has failed to set forth a proper *prima facie* case of anticipation under 35 U.S.C. § 112 paragraph 6. Additionally, the claim as amended provides further recitation not found in the cited reference. Thus, claim 32 overcomes the Examiner's rejection under 35 U.S.C. § 102(e). Reconsideration and an early indication of allowance is respectfully requested.

Claims 33-36 depend from claim 32 and include the recitations of claim 32 by their dependency. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed. Accordingly, claims 33-36 now overcome the Examiner's rejection under 35 U.S.C. § 102(e).

Further regarding claim 33, the Examiner has not cited equivalent structures, material, or acts described therein "for setting the non executable indication is done for a page holding the data for a data access" as recited in claim 33. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claim 34, the Examiner has not cited equivalent structures, material, or acts described therein "for checking the non executable indication" as recited in claim 34. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claim 35, the Examiner has not cited equivalent structures, material, or acts described therein "for checking the non executable indication; and ... for disallowing an instruction-buffer load based on the non executable setting" as recited in claim 35. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Further regarding claim 36, the Examiner has not cited equivalent structures, material, or acts described therein "for setting the non executable indication to "on" for a page holding the data for the data access address if a write indication is set for that page" as recited in claim 36. Accordingly, the Kolichtchak reference fails to disclose the invention as claimed, and this claim appears to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

§103 Rejection of the Claims

A. Rejection: Claims 3, 4, and 14-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kolichtchak (US 2003/0014667).

B. Response: Applicant's recitation of the law and the MPEP in the response filed February 27, 2006 regarding obviousness is incorporated herein by reference.

Claims 3 and 4 depend from claim 1 and include the limitations of claim 1 by their dependency. Therefore, the Kolichtchak reference fails to teach or suggest all the claim limitations of claims 3 and 4. Claims 3 and 4 also include further limitations to vector TLBs or scalar TLBs not found in Kolichtchak. Applicant challenges the Examiner's assertion that having dedicated vector TLBs and dedicated scalar TLBs and then combining such structures with Kolichtchak is obvious, and respectfully **requests, under MPEP 2144.03,** that the Examiner provide a reference explicitly showing separate vector TLBs and/or scalar TLBs, **and provide a motivation provided in the prior art for a combination of such a reference with Kolichtchak.** ***Applicant also made this request in the prior response, and it was ignored.***

It is improper to use the present application as motivation. Applicant does not understand the Examiner's assertion that the prior art combination asserted provides "for the desirable purpose of providing accuracy and data protection." Having separate scalar and vector caches provides performance. How does it provide accuracy or data protection? Applicant respectfully submits that the Examiner has failed to provide the required prima facie case under MPEP 2106:

> "Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered. See, e.g., *Diamond v. Diehr*, 450 U.S. at 188-89, 209 USPQ at 9 ("In determining the eligibility of respondents' claimed process for patent protection under 101, their claims must be considered as a whole. It is inappropriate to dissect the claims into old and new elements and then to ignore the presence of the old elements in the analysis. ...")"

These claims appear to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

Claims 14 and 15 depend from claim 10 and include the limitations of claim 10 by their dependency. Applicant again requests, under MPEP 2144.03, that the Examiner provide a

reference explicitly showing separate vector TLBs and/or scalar TLBs, and provide a motivation provided in the prior art for a combination of such a reference with Kolichtchak. These claims appear to be in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

In addition, the Examiner rejected claims 3, 4, 14 and 15 based solely on the Kolichtchak reference. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103(a) since not all of the recited elements of the claims are found in the Kolichtchak reference. Since all the elements of the claims are not found in the Kolichtchak reference, Applicant requests that the Examiner cite a reference that includes the (x) executable/non-executable indicator and the specific ways it operates. In the alternative, Applicant requests that the Examiner place an affidavit of personal knowledge in the file for any elements the Examiner has failed to produce a reference clearly showing an element or elements. Still another alternative is that the Examiner indicates any taking official notice of the missing elements. Applicant respectfully objects to the reason set forth for obviousness set forth in the Office Action of September 27, 2005 or to any taking of official notice with a single-reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, respectfully requests one of the above-suggested responses from the Examiner.

For all of the reasons set forth above, claims 3, 4, 14 and 15 appear in condition for allowance. Reconsideration and an early indication of allowance are respectfully requested.

New claims 37-42 have been added as variations to more fully describe the claimed invention. These appear to be within the subject matter searched. Consideration of these claims and an early indication of allowance are respectfully requested

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Charles A. Lemaire (952)-278-3501 or Richard E. Billion (612) 373-6977 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CANDIS BUENDING

Name

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